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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,609	09/15/2003	Chih-Yang Pai	TSM03-0146	2342
43859	7590	08/09/2006	EXAMINER	
SLATER & MATSIL, L.L.P. 17950 PRESTON ROAD, SUITE 1000 DALLAS, TX 75252			LE, THAO X	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/662,609	PAI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 27 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 24-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 24-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date: _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date: _____  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Response to Amendment*

1. Newly submitted claims 34-43 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: The base claims 34 and 39 are the method of forming a transistors comprising a multiple layers gate electrode.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 34-43 withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 24-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly added limitation "wherein the logic gate oxide and the first doped polysilicon laver form a first transistor and the cell gate

oxide, the first doped polysilicon layer, and the second polysilicon layer from a second transistor" is not described in the original specification. Because as shown in fig. 3m the logic oxide layer 341 and the second doped polysilicon 344 may or would a transistor in the peripheral region 308 while fig. 3n fails to show such arrangement. It is not clear in fig. 3n the second doped polysilicon 344 still remains as the gate electrode of a transistor in the peripheral region 308. There is no such explicit indication in any drawings.

Thus, the newly added limitation s is not being considered.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 24 are rejected under 35 U.S.C. 102(b) as being anticipated by US 55903035 to Wu et al.

Regarding claim 24, Wu discloses a method of forming a semiconductor devise, the method comprising: forming a cell gate oxide 76", fig. 11, column 5 line 35, in a cell region; forming a logic gate oxide 66', column 5 line 65, in a periphery region, forming a first doped polysilicon layer 78, column 5 lines 37, on the cell gate oxide 76"; and forming a second polysilicon layer 74', col. 5 line 40 or claim 1, the second polysilicon layer being in contact with the logic gate oxide 66' in the peripheral region and in

contact with a major surface of the first doped polysilicon layer 78 in the cell region, fig.

11.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 25-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 55903035 to Wu et al. in view of US 5668035 to Fang et al.

Regarding claims 25-26, 30-33, Wu does not disclose the method wherein the second polysilicon layer 74" positioned above the cell gate oxide 76" is a p-type doped polysilicon, the second polysilicon layer is doped with a material selected from the group consisting essentially of phosphorous, nitrogen, arsenic, and antimony, and further

comprising the step of doping the second polysilicon layer located above the logic gate oxide with an n-type dopant.

However, Fang discloses the method wherein the second polysilicon layer 20 positioned above the cell gate oxide 14, fig. 6, is a p-type doped polysilicon, the second polysilicon layer is doped with a material selected from the group consisting essentially of phosphorous, nitrogen, arsenic, and antimony, column 4 line 62, and further comprising the step of doping the second polysilicon layer 20 located above the logic gate oxide with an n-type dopant, column 3 lines 25-30. Obviously, Fang discloses layer 20 can be doped with either N-type or P-type dopant. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the doping teaching of Fang with Wu's method, because such P or N type silicon doping is typical in the art to create a conductor for intended purpose.

Regarding claims 27-28, Wu does not discloses the method wherein the step of forming a first polysilicon layer 78 is performed by depositing by furnace an in-situ doped polysilicon wherein depositing by furnace is performed at a temperature of about 550°C to about 600°C.

However, Fang discloses the method wherein the step of forming a first polysilicon layer 16 is performed by depositing by furnace an in-situ doped polysilicon, column 4 line 16, wherein depositing by furnace is performed at a temperature of about 550°C to about 600°C, column 4 line 13. At the time the invention was made; it would have been obvious to one of ordinary skill in the art

to use the teaching method of Fang with Wu's method, because such silicon deposition is typical in the art.

Regarding claim 29, Wu discloses wherein the second polysilicon layer 74" is formed of polysilicon, claim 1. Obviously, such layer can be an undoped polysilicon layer as it being disclosed by Fang, column 4 lines 10-15.

### ***Response to Arguments***

9. Applicant's arguments with respect to claims 24-33 have been considered but are moot in view of the new ground(s) of rejection in section 2.

### ***Conclusion***

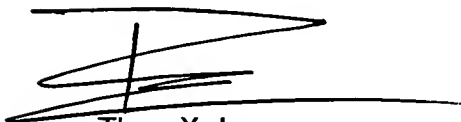
10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, consisting of a stylized 'T' followed by a horizontal line and a vertical line intersecting it.

Thao X. Le  
07 Aug. 2006